

### REMARKS

Claims 1-2, 4-7, and 9-36 are pending in the application.

Claims 1-7 and 9-36 have been rejected.

Claim 3 has been canceled.

Claims 4, 5, 14-18, 22, 24, 27, 30, 33, and 36 have been amended. Support for the amendments to these claims can be found, at least, in paragraph 23 of the specification.

### Objections

In the Office Action mailed November 1, 2006 (hereinafter referred to as "Office Action"), the Examiner objected to the specification for failing to provide proper antecedent basis for the phrase "tangible computer readable medium." Office Action, p. 2. However, paragraph 59 of the specification gives a variety of different examples of tangible computer readable media. Accordingly, Applicants respectfully assert that this objection is moot.

### Rejection of Claims under 35 U.S.C. §112

Claims 33-35 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Office Action, p. 3. The Examiner states: "a person of skill in the art would not be able to ascertain the metes and bounds of the claimed invention, specifically, for the term 'a tangible computer readable medium.'" Office Action, pages 3-4. Applicant notes that one of ordinary skill in the art could easily ascertain that "a tangible computer readable medium" is a computer readable medium that is also tangible. Several examples of such computer readable media are presented in specification (e.g., in paragraph 59). Accordingly, Applicant respectfully asserts that this claim language is definite and requests the withdrawal of this rejection.

Rejection of Claims under 35 U.S.C. §101

Claims 33-35 stand rejected under 35 U.S.C. §101 as being directed to non-statutory subject matter. The Examiner pointed out that claims 30-35 (it is unclear whether claims 30-32 are actually being rejected or not) might not be limited to tangible embodiments. Office Action, p. 3. With respect to claims 30-32, Applicant notes that these claims require a processor, which is inherently tangible. Accordingly, Applicants assert that this rejection does not appear to apply to claims 30-32. Additionally, Applicant notes that independent claim 33 (and thus also dependent claims 34-35) explicitly recite the word “tangible.” Applicant therefore asserts that this rejection has been overcome.

Rejection of Claims under 35 U.S.C. §102

Claims 1, 3-7 and 9-36 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kashima et al. (USPN: 5,485,598) hereinafter referred to as “Kashima.” Applicant respectfully traverses this rejection.

As amended, claim 36 recites: “maintaining a first cache, wherein said maintaining is performed by one of an upper-level system and a lower-level storage module,” “cloning information stored in a first unit of storage into a second unit of storage, wherein said first cache comprises said first unit of storage and a second cache comprises said second unit of storage,” and “accessing said second cache, wherein said accessing is performed by the other of said upper-level system and said lower-level storage module.” Kashima does not teach these features of claim 36. In particular, the cited portions of Kashima do not teach a system in which information is copied from a cache maintained by either an upper-level system or a lower-level storage module into another cache, which is then accessed by the other one of the upper-level system or lower-level storage module.

In the Office Action, the Examiner equates the “upper-level system” of claim 36 with the CPU of Kashima, while also equating the “lower-level system” of the prior version of claim 36 with the OS of Kashima. Office Action, p. 4. Alternatively, the

Examiner states that both the upper-level system and the lower-level system with computer 10 of Kashima. Office Action, p. 14.

The cited art teaches a system in which the old data cache can be part of the main memory system (e.g., as shown in FIGs. 8 and 11 of Kashima) or part of a disk array (e.g., as shown in FIGs. 4 and 14 of Kashima). Both the CPU and the OS are part of the computer 10. Neither the CPU nor the OS is a “lower-level storage module,” as recited in the current version of claim 36. Computer 10 of Kashima is also clearly not a lower-level storage module. Accordingly, the cited art fails to teach or suggest the scenario claimed in amended claim 36, which involves a lower-level storage module maintaining or having access to a cache.

For at least the foregoing reasons, the cited art fails to teach or suggest amended claim 36 and its dependent claims 1, 4-7, and 9-13. Claims 14-36 are patentable over the cited art for similar reasons.

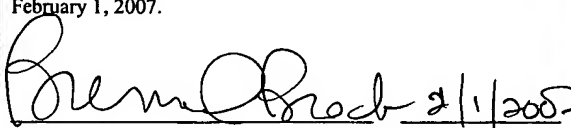
*Rejection of Claims under 35 U.S.C. §103*

Claim 2 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Kashima. Applicant respectfully traverses this rejection, for at least the foregoing reasons presented above with respect to claim 36.

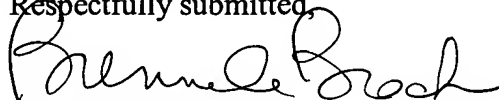
Further with respect to claim 2, Applicant notes that, regardless of whether it is well-known in the art to integrate certain types of caches, it is not well known to integrate caches such as those described in claim 2. In particular, claim 2 describes a single cache that includes both a first cache and a second cache, the latter of which is maintained by either an upper-level system or a lower-level system and also able to be accessed by the other of the upper-level system or the lower-level system, as described in claim 36 (from which claim 2 depends). While the rejection addresses the general concept of combining two caches, no teachings or suggestions have been provided as to why one would integrate the two caches described in claim 36, which have specifically claimed functionality (e.g., the ability of the second cache to be maintained by one system while also capable of being accessed by another system).

**CONCLUSION**

In view of the amendments and remarks set forth herein, the application and the claims therein are believed to be in condition for allowance without any further examination and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is invited to telephone the undersigned at 512-439-5087.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop RCE, COMMISSIONER FOR PATENTS, P. O. Box 1450, Alexandria, VA 22313-1450, on February 1, 2007.	
	2/1/2007
Attorney for Applicant(s)	Date of Signature

Respectfully submitted,



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